UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,368	05/09/2005	Jun Ogura	05274/LH	2923

1933 7590 04/01/2008
FRISHAUF, HOLTZ, GOODMAN & CHICK, PC
220 Fifth Avenue
16TH Floor
NEW YORK, NY 10001-7708

EXAMINER	
CROW, ROBERT THOMAS	

ART UNIT	PAPER NUMBER
1634	

MAIL DATE	DELIVERY MODE
04/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,368	OGURA ET AL.	
	Examiner	**Art Unit**	
	Robert T. Crow	1634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,8,10-13 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-5, 8, 10-13, and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/8/2008*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 February 2008 has been entered.

Status of the Claims

2. This action is in response to papers filed 8 February 2008 in which the specification and claims 1, 5, 8, and 10 were amended, claims 6-7 and 9 were canceled, and new claims 18-21 were added. All of the amendments have been thoroughly reviewed and entered.

The previous rejections under 35 U.S.C. 112, second paragraph, are withdrawn in view of the amendments.

The previous rejections under 35 U.S.C. 102(b) and 35 U.S.C. 103(a) not reiterated below are withdrawn in view of the amendments. Applicant's arguments have been thoroughly reviewed and are addressed following the rejections necessitated by the amendments.

Claims 1, 4-5, 8, 10-13, and 17-21 are under prosecution.

Information Disclosure Statement

3. The Information Disclosure Statement filed 8 February 2008 is acknowledged. However, only the Abstracts of the documents listed are being considered because English language translations of the remainder of the documents have not been provided.

In addition, it is noted that while the search reports supplied by Applicant are not listed on the Information Disclosure Statement, they have been considered. Further, Applicant has also submitted

documents JP 9-504910 and JP 7-508831. These documents are not listed in the Information Disclosure Statement, nor are they in English. Therefore, they have not been considered.

4. The rejections presented below are new rejections necessitated by the amendments.

Claim Rejections - 35 USC § 112, First Paragraph

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 8, 10-13, and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. **<u>This is a new matter rejection</u>**. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 10, upon which claims 11-13 and 17 depend, and claim 8 each recite a "means for applying a negative voltage to the light-transmissive top gate electrode in a charge storage period" in lines 11-12 of claim 8 and in lines 12-13 of claim 10, and also each recite a "means for applying a positive voltage and a ground potential to the transparent conductive layer" in the last 2 lines of claim 8 and in lines 22-23 of claim 10. A review of the specification yields no recitation of either a "means for applying a negative voltage to the light-transmissive top gate electrode in a charge storage period" or a "means for applying a positive voltage and a ground potential to the transparent conductive layer." Applicant has cited page 80 line 18-page 81, line 6 for support of this amendment. However, the citation merely recites impression of a positive voltage to a conductive layer, and "top gate driver 11, the bottom gate driver 12, the data driver 13, and the driving circuit 10…." Thus, the broadly claimed "means for applying a negative voltage to the light-transmissive top gate electrode in a charge storage period" and "means for applying a positive voltage and a ground potential to the transparent conductive layer" encompass

embodiments other than a top gate driver, bottom gate driver, data driver, and a driving circuit, and therefore constitute new matter.

Claim Rejections - 35 USC § 112, Second Paragraph

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8, 10-13 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 10-13 and 17 are indefinite in claims 8 and 10, each of which recites the limitation "the light transmissive top gate electrode" in lines 11-12 of claim 8 in lines 12-13 of claim 10, and the recitation "the transparent conductive layer" at the end of claim 8 and in line 23 of claim 10. The singular recitations of "the light transmissive top gate electrode" and "the transparent conductive layer" lack antecedent basis because the claims comprising a plurality of light transmissive top gate electrodes and light transmissive top gate electrodes because each singular recitation is a part of the plurality of photoelectric elements. It is suggested the claims be amended to reflect proper antecedent basis.

Claim Interpretation- 35 USC § 112, Sixth Paragraph

9. The following is a quotation of the sixth paragraph of 35 U.S.C. 112:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

10. Applicant has invoked 35 USC § 112 Sixth Paragraph in the limitation "means for applying a negative voltage to the light-transmissive top gate electrode in a charge storage period" in lines 11-12 of

claim 8 and in lines 12-13 of claim 10, and in the limitation "means for applying a positive voltage and a ground potential to the transparent conductive layer" in the last 2 lines of claim 8 and in lines 22-23 of claim 10. While the limitations meet the three-prong analysis for consideration under 35 USC § 112 Sixth Paragraph, the limitation "means for applying a negative voltage to the light-transmissive top gate electrode in a charge storage period" and the limitation "means for applying a positive voltage and a ground potential to the transparent conductive layer" are not being treated under 35 USC 112, sixth paragraph because the specification does not provide a **limiting definition** of the **structural** elements that define the **structures** of the means that provide the various functions found in the claims. Thus, the claims are given the broadest reasonable interpretation consistent with the specification (*In re Hyatt*, 211 F.3d1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) (see MPEP 2111 [R-1]).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 1, 5, 8, 10-13, 17, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollis et al (U.S. Patent No. 5,846,708, issued 8 December 1998) in view of Iihama (U.S. Patent Application Publication No. US 200390014530 A1, published 7 February 2002), and as evidenced by Garvison et al (U.S. Patent No. 6,465,724 B1, issued 15 October 2002).

Regarding claim 1, Hollis et al teach an optical DNA sensor. In a single exemplary embodiment, Hollis et al teach a device comprising a solid imaging device, in the form of an underlying CCD array having an array test sites formed thereon (Figure 15 and column 3, lines 50-55). Each test site of the array has DNA probes fixed (i.e., attached) thereon (column 4, lines 25-65). The probes at each test site are different (column 3, lines 1-8); thus, the sensor comprises a plurality of types of DNA probes each including a different nucleotide sequence. The CCD array comprises a plurality (i.e., at least 2, Figure 15) of photoelectric elements arranged on a substrate (Figure 15).

It is noted that a reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. *Merck & Co. v. Biocraft Laboratories,* 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989). See also *Upsher-Smith Labs. v. Pamlab, LLC,* 412 F.3d 1319, 1323, 75 USPQ2d 1213, 1215 (Fed. Cir. 2005)(reference disclosing optional inclusion of a particular component teaches compositions that both do and do not contain that component); Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998) (The court held that the prior art anticipated the claims even though it taught away from the claimed invention. “The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed.”). Thus, the teaching of Hollis et al that the material to which the DNA probes are fixed **may** be light-transmissive (column 9, lines 15-32) encompasses the alternate embodiment wherein the material is **not** light-transmissive; i.e., absorbs exciting light. See MPEP § 2123 [R-5].

While Hollis et al teach the photosensor array comprises gate electrodes 220 provided in the solid state imaging device and other layers (Figure 15), Hollis et al do not explicitly teach an exciting light absorbing layer and a conductive layer.

However, Iihama teaches a two dimensional reading apparatus (Abstract) in the form of a photosensor array (paragraph 0003), wherein each photosensor of the array comprises bottom gate electrode 22, conductive layer 23 formed of indium tin oxide (i.e., ITO), and an uppermost protective layer 27 of amorphous silicon (Figure 25 and paragraphs 0050-0054 and 0111-0113). Garvison et al teach amorphous silicon absorbs UV and visible light (column 14, line 65-column 15, line 1). Thus, the protective layer of amorphous silicon is a light absorbing layer. Iihama also teaches the photosensors have the added advantage of markedly suppressing the malfunction of reading and breakage of the device (Abstract). Thus, Iihama teaches the known technique of using the claimed photosensor array.

It is noted that the courts have held that "while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function." *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). In addition, "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch &Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original). Therefore, the various uses recited in claim 1 (e.g., absorbing exciting light, generating electron hole pairs, and discharging charges) fail to define additional structural elements to the device of claim 1. Because the prior art teaches the structural elements of claim 1, the claim is obvious over the prior art. See MPEP § 2114.

It would therefore have been obvious to a person of ordinary skill in the art at the time the claimed invention was made to have modified the sensor comprising the plurality of photosensors as taught by Hollis et al with the photosensor array of Iihama to arrive at the instantly claimed invention with a reasonable expectation of success. The ordinary artisan would have been motivated to make the modification because said modification would have resulted in a sensor having the added advantage of

markedly suppressing the malfunction of reading and breakage of the device as explicitly taught by Iihama (Abstract). In addition, it would have been obvious to the ordinary artisan that the known technique of using the photosensor array of Iihama could have been applied to the sensor of Hollis et al with predictable results because the photosensor array of Iihama predictably results in an array of viable photosensors.

Regarding claim 5, Hollis et al teach an optical DNA sensor. In a single exemplary embodiment, Hollis et al teach a device comprising a solid imaging device, in the form of an underlying CCD array having an array test sites formed thereon (Figure 15 and column 3, lines 50-55). Each test site of the array has DNA probes fixed (i.e., attached) thereon (column 4, lines 25-65). The probes at each test site are different (column 3, lines 1-8); thus, the sensor comprises a plurality of types of DNA probes each including a different nucleotide sequence The DNA probes are fixed on a layer of material (column 9, lines 15-32). The CCD array comprises a plurality (i.e., at least 2, Figure 15) of photoelectric elements arranged on a substrate (Figure 15).

As noted above, a reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. Thus, the teaching of Hollis et al that the material to which the DNA probes are fixed **may** be light-transmissive (column 9, lines 15-32) encompasses the alternate embodiment wherein the material is **not** light-transmissive; i.e., absorbs exciting light.

While Hollis et al teach the photosensor array comprises gate electrodes 220 provided in the solid state imaging device and other layers (Figure 15), Hollis et al do not explicitly teach an exciting light absorbing layer and a conductive layer.

However, Iihama teaches a two dimensional reading apparatus (Abstract) in the form of a photosensor array (paragraph 0003), wherein each photosensor of the array comprises bottom gate electrode 22, conductive layer 23 formed of indium tin oxide (i.e., ITO), and an uppermost protective layer 27 of amorphous silicon (Figure 25 and paragraphs 0050-0054 and 0111-0113). Garvison et al teach

amorphous silicon absorbs UV and visible light (column 14, line 65-column 15, line 1). Thus, the protective layer of amorphous silicon is a light absorbing layer. Iihama also teaches the photosensors have the added advantage of markedly suppressing the malfunction of reading and breakage of the device (Abstract). Thus, Iihama teaches the known technique of using the claimed photosensor array.

As noted above, apparatus claims cover what a device *is*, not what a device *does*. Therefore, the various uses recited in claim 5 (e.g., absorbing exciting light, generating electron hole pairs, and discharging charges) fail to define additional structural elements to the device of claim 5. Because the prior art teaches the structural elements of claim 5, the claim is obvious over the prior art.

It would therefore have been obvious to a person of ordinary skill in the art at the time the claimed invention was made to have modified the sensor comprising the plurality of photosensors as taught by Hollis et al with the photosensor array of Iihama to arrive at the instantly claimed invention with a reasonable expectation of success. The ordinary artisan would have been motivated to make the modification because said modification would have resulted in a sensor having the added advantage of markedly suppressing the malfunction of reading and breakage of the device as explicitly taught by Iihama (Abstract). In addition, it would have been obvious to the ordinary artisan that the known technique of using the photosensor array of Iihama could have been applied to the sensor of Hollis et al with predictable results because the photosensor array of Iihama predictably results in an array of viable photosensors.

Regarding claim 8, Hollis et al teach an optical DNA sensor. In a single exemplary embodiment, Hollis et al teach a solid imaging device in the form of a CCD array, which comprises a plurality of photoelectric elements arranged apart from each other (i.e., Figure 15). The elements are on substrate that is transparent (column 10, lines 5-6), and has a bottom gate electrode having a shading property; namely, gate electrodes of tungsten (column 9, lines 15-65), which has a shading property because it is not entirely transparent. Each test site of the array has DNA probes fixed (i.e., attached) thereon (column 4, lines 25-65). The probes at each test site are different (column 3, lines 1-8); thus, the sensor comprises a plurality

of types of DNA probes each including a different nucleotide sequence. The DNA probes are fixed on a dielectric multilayered film; namely, a first layer of material and an upper protective layer of silicon nitride are on the substrate, wherein the silicon nitride is transparent and has the probes thereon (column 9, lines 15-32).

While Hollis et al teach the photosensor array comprises gate electrodes 220 provided in the solid state imaging device and other layers (Figure 15), Hollis et al do not explicitly teach the layered gate electrode structure of the claim, a plurality of means for applying a voltage, or a transparent conductive layer.

However, Iihama teaches a two dimensional reading apparatus (Abstract) in the form of a photosensor array (paragraph 0003), wherein each photosensor of the array comprises bottom gate electrode 22, semiconductor layer 11, which is light sensitive, top gate electrode 21, which transmits visible light (Figure 1 and paragraphs 0050-0054). Each photosensor further comprises conductive layer 23 formed of indium tin oxide (i.e., ITO), which is transparent. Iihama et al also teach a voltage is applied to top gate electrode 21 (paragraph 0054) via a gate driver (Figure 3) and that a voltage is applied to bottom gate electrode 22 (paragraph 0054) via a bottom gate driver (Figure 3). Thus, the two means for applying voltages of Iihama are in accordance with the example presented on page 80 line 18-page 81, line 6 of the instant specification. The application of negative voltage to the top gate electrode is also taught by Iihama (paragraph 0064), as is the application of positive voltage to the bottom gate electrode (paragraph 0067) which utilizes the same voltage source as the semiconductor layer (paragraph 0054). Iihama also teaches the photosensors have the added advantage of markedly suppressing the malfunction of reading and breakage of the device (Abstract). Thus, Iihama teaches the known technique of using the claimed photosensor array

It would therefore have been obvious to a person of ordinary skill in the art at the time the claimed invention was made to have modified the sensor comprising the plurality of photosensors as taught by Hollis et al with the photosensor array of Iihama to arrive at the instantly claimed invention

with a reasonable expectation of success. The ordinary artisan would have been motivated to make the modification because said modification would have resulted in a sensor having the added advantage of markedly suppressing the malfunction of reading and breakage of the device as explicitly taught by Iihama (Abstract). In addition, it would have been obvious to the ordinary artisan that the known technique of using the photosensor array of Iihama could have been applied to the sensor of Hollis et al with predictable results because the photosensor array of Iihama predictably results in an array of viable photosensors.

Regarding claim 10, Hollis et al teach an DNA reading apparatus. In a single exemplary embodiment, Hollis et al teach a solid imaging device in the form of a CCD array, which comprises a plurality of photoelectric elements arranged apart from each other (i.e., Figure 15). The elements are on substrate that is transparent (column 10, lines 5-6), and has a bottom gate electrode having a shading property; namely, gate electrodes of tungsten (column 9, lines 15-65), which has a shading property because it is not entirely transparent. Each test site of the array has DNA probes fixed (i.e., attached) thereon (column 4, lines 25-65). The probes at each test site are different (column 3, lines 1-8); thus, the sensor comprises a plurality of types of DNA probes each including a different nucleotide sequence. The DNA probes are fixed on a dielectric multilayered film; namely, a first layer of material and an upper protective layer of silicon nitride are on the substrate, wherein the silicon nitride is transparent and has the probes thereon (column 9, lines 15-32).

While Hollis et al teach the photosensor array comprises gate electrodes 220 provided in the solid state imaging device and other layers (Figure 15), Hollis et al do not explicitly teach the layered gate electrode structure of the claim, a plurality of means for applying a voltage, a transparent conductive layer, or a light irradiation member irradiating the rear surface.

However, Iihama teaches a two dimensional reading apparatus (Abstract) in the form of a photosensor array (paragraph 0003), wherein each photosensor of the array comprises bottom gate electrode 22, semiconductor layer 11, which is light sensitive, top gate electrode 21, which transmits

visible light (Figure 1 and paragraphs 0050-0054). Each photosensor further comprises conductive layer 23 formed of indium tin oxide (i.e., ITO), which is transparent. Iihama et al also teach a voltage is applied to top gate electrode 21 (paragraph 0054) via a to gate driver (Figure 3) and that a voltage is applied to bottom gate electrode 22 (paragraph 0054) via a bottom gate driver (Figure 3). Thus, the two means for applying voltages of Iihama are in accordance with the example presented on page 80 line 18-page 81, line 6 of the instant specification. The application of negative voltage to the top gate electrode is also taught by Iihama (paragraph 0064), as is the application of positive voltage to the bottom gate electrode (paragraph 0067) which utilizes the same voltage source as the semiconductor layer (paragraph 0054). Iihama teaches the apparatus further comprises back light system 30, which is a light irradiation member which irradiated light toward a rear surface of the imaging device (Figure 14 and paragraph 0074). Iihama also teaches the photosensors have the added advantage of markedly suppressing the malfunction of reading and breakage of the device (Abstract). Thus, Iihama teaches the known technique of using the claimed photosensor array and irradiation member..

It would therefore have been obvious to a person of ordinary skill in the art at the time the claimed invention was made to have modified the sensor comprising the plurality of photosensors as taught by Hollis et al with the photosensor array an irradiation member of Iihama to arrive at the instantly claimed invention with a reasonable expectation of success. The ordinary artisan would have been motivated to make the modification because said modification would have resulted in a sensor having the added advantage of markedly suppressing the malfunction of reading and breakage of the device as explicitly taught by Iihama (Abstract). In addition, it would have been obvious to the ordinary artisan that the known technique of using the photosensor array of Iihama could have been applied to the sensor of Hollis et al with predictable results because the photosensor array of Iihama predictably results in an array of viable photosensors.

Regarding claim 11, the apparatus of claim 10 is discussed above. Iihama teaches the light irradiation member is below the substrate (Figure 14 and paragraph 0074). Therefore, modification of the

apparatus of Hollis et al with the photosensor array and light irradiation member of Iihama results in the disposition of the light irradiation member below the substrate.

Regarding claims 12-13 and 17, the sensor of claim 11 is discussed above. As noted above apparatus claims cover what a device *is*, not what a device *does*. Therefore, the various uses recited in claims 12-13 and 17 (e.g., irradiating a phosphor [i.e., claim 12], or exciting a fluorescent substance [i.e., claims 13 and 17]) fail to define additional structural elements to the device of claim 11. Because the prior art teaches the structural elements of claim 11, claims 12 and 13-17 are also obvious over the prior art.

Regarding claim 20, the sensor of claim 1 is discussed above. Iihama teaches the application of negative voltage to the top gate electrode (paragraph 0064), and the application of positive voltage to the bottom gate electrode (paragraph 0067) which utilizes the same voltage source as the semiconductor layer (paragraph 0054). Therefore, modification of the apparatus of Hollis et al with the photosensor array and light irradiation member of Iihama results in a device capable of applying a positive voltage to the semiconductor layer.

In addition, as noted above apparatus claims cover what a device *is*, not what a device *does*. Therefore, the various uses recited in claim 20 (e.g., applying a positive voltage) fail to define additional structural elements to the device of claim 20. Because the prior art teaches the structural elements of claim 20, the claim is obvious over the prior art.

Regarding claim 21, the sensor of claim 1 is discussed above. Iihama also teaches an additional protective insulated layer between the conductive layer and the plurality of photoelectric elements; namely, protective insulating film 20 (Figure 25 and paragraphs 0050-0054). Therefore, modification of the apparatus of Hollis et al with the photosensor array and light irradiation member of Iihama results in an additional protective insulated layer between the conductive layer and the plurality of photoelectric elements.

14. Claims 4 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollis et al (U.S. Patent No. 5,846,708, issued 8 December 1998) in view of Iihama (U.S. Patent Application Publication No. US 200390014530 A1, published 7 February 2002), and as evidenced by Garvison et al (U.S. Patent No. 6,465,724 B1, issued 15 October 2002) as applied to claim 1 above, and further in view of Iwasa (U.S. Patent No. 5,381,028, issued 10 January 1995).

Regarding claim 4, the sensor of claim 1 is discussed above in Section 13.

While Hollis et al further teach semiconductor layers (column 14, lines 40-50) and transistors integrated into the substrate (column 20, lines 20-35), neither Hollis et al nor Iihama explicitly teach field effect transistor type photoelectric elements.

However, Iwasa teaches MOS field effect transistors having a semiconductor layer of polysilicon (Abstract), which generated electric charges in response to light in accordance with the example on page 49 of the instant specification. Iwasa also teaches the MOS field effect transistors have the added advantage of fewer defects and utility in the miniaturization of devices (column 1, line 65-column 2, line 3). Thus, Iwasa teaches the known technique of using MOS field effect transistors having a semiconductor layer.

It would therefore have been obvious to a person of ordinary skill in the art at the time the claimed invention was made to have modified the DNA sensor of Hollis et al in view of Iihama with the field effect transistors of Iwasa with a reasonable expectation of success. The ordinary artisan would have been motivated to make such a modification because said modification would have resulted in a DNA sensor having the added advantage of fewer defects in a miniaturized device as explicitly taught by Iwasa (column 1, line 65-column 2, line 3). In addition, it would have been obvious to the ordinary artisan that the known technique of using the MOS field effect transistors having a semiconductor layer of Iwasa could have been applied to the sensor of Hollis et al in view of Iihama with predictable results because the MOS field effect transistors having a semiconductor layer of Iwasa predictably result in transistors usable with gate electrodes.

Regarding claim 18, the sensor of claim 4 is discussed above. Iihama teaches each photosensor of the array comprises bottom gate electrode 22, semiconductor layer 11, which is light sensitive, top gate electrode 21, which transmits visible light (Figure 1 and paragraphs 0050-0054). Therefore, modification of the apparatus of Hollis et al with the photosensor array and light irradiation member of Iihama results in the claimed gate electrodes.

Regarding claim 19, the sensor of claim 18 is discussed above. Iihama teaches the application of negative voltage to the top gate electrode (paragraph 0064), and the application of positive voltage to the bottom gate electrode (paragraph 0067) which utilizes the same voltage source as the semiconductor layer (paragraph 0054). Therefore, modification of the apparatus of Hollis et al with the photosensor array and light irradiation member of Iihama results in a device capable of applying a negative voltage to the top gate electrode.

In addition, as noted above apparatus claims cover what a device *is*, not what a device *does*. Therefore, the various <u>uses</u> recited in claim 19 (e.g., applying a negative voltage) fail to define additional structural elements to the device of claim 19. Because the prior art teaches the <u>structural</u> elements of claim 19, the claim is obvious over the prior art.

Response to Arguments

15. Applicant's arguments with respect to the previous rejections of the claims have been considered but are moot in view of the new ground(s) of rejection necessitated by the amendments.

Conclusion

16. No claim is allowed.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert T. Crow whose telephone number is (571)272-1113. The examiner can normally be reached on Monday through Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ram Shukla can be reached on (571) 272-0735. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert T. Crow/
Examiner, Art Unit 1634

/Diana B. Johannsen/
Primary Examiner, Art Unit 1634

Robert T. Crow
Examiner
Art Unit 1634